DOTTORATO DI RICERCA IN FISICA

CORSO DI SEMINARI DI INDIRIZZO NUCLEARE

A.A. 2007/2008

Lunedì 14 gennaio 2008 alle ore 15.00 in Sala Riunioni il

Prof. Dario Crosetto

(The Crosetto Foundation, De Soto, Texas)

Terrà una lezione dal titolo:

METHOD AND APPARATUS FOR EXTENDING PROCESSING TIME IN ONE PIPELINE STAGE

Abstract: A single channel or multi-channel system that requires the execution time of a pipeline stage to be extended to a time longer than the time interval between two consecutive input data. Each analog or digital circuit (or processor) has at least one input and one output port connected to an internal or external "bypass switch"_ (or multiplexer). The data arriving from the input can be sent either to the internal circuit (or processor), or can be sent to the output with no processing by the circuit (or processor) through a register that requires at least one clock cycle to move the data from the input to the output of the register. For a stage of one channel requiring an algorithm execution time twice the time interval between two consecutive input data, two circuits are required to be cascaded and interconnected by the internal or external "bypass switch._ Data and results flow synchronously from the first circuit at the input of the system, through the "bypass switches" of the cascaded circuits, to the last at the output. The hardware approach of the implementation of the layout of the "bypass switches"_ with respect to the circuits is such that maximum input data rate is achieved and is independent of the number of cascaded circuits used. The number of cascaded circuits is proportional to the algorithm execution time.

Gli studenti di Dottorato e tutti gli interessati sono cordialmente invitati

Titolare del Corso
Prof. Sergio P. Ratti